ISSN: 0976-3376

Available Online at http://www.journalajst.com

ASIAN JOURNAL OF SCIENCE AND TECHNOLOGY

Asian Journal of Science and Technology
Vol. 08, Issue, 04, pp.4704-4707, April, 2017

RESEARCH ARTICLE

TOTAL REDUCTION OF LEAKAGE POWER THROUGH COMBINED EFFECT OF SLEEP STACK AND VARIABLE BODY BIASING TECHNIQUE

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ARTICLE INFO

Article History:
Received 10th January, 2017
Received in revised form
17th February, 2017
Accepted 13th March, 2017
Published online 30th April, 2017

Key words:

ITRS, SSVBB, Sleep stack,
Body bias, dual V_{th}.

ABSTRACT

Leakage power consumption has become a major concern for VLSI circuit designers. Leakage power will become dominant by the year 2020 as per the report of ITRS. I propose the new approach, named sleepy stack with variable body biasing (SSVBB), which reduces the leakage current thereby saving the state of art. It uses traditional sleep transistors which are placed parallel to PMOS/NMOS between the pull up/pull down device and VDD/GND. Dual V_{th} can be also be applied to reduce sub threshold leakage current. It achieves exact same power reduction as zigzag approach along with saving the logic state of the circuit. Based on the experiments with the inverter as the benchmark circuit, it is found that there is 48% of reduction in delay but with the sacrifice of area. For the application which requires long idle/standby time while maintaining the logic state, the stack sleep with variable body biasing can be used.

INTRODUCTION

Aggressive scaling of CMOS circuits with respect to feature size and threshold voltage has lead to dramatic increase in leakage current. Another possible dominant leakage power is gate oxide leakage and reverse bias band to band tunnelling, which contribute to more than 25% of total power consumption. Thus leakage power increases exponentially with the reduction in the feature size. With increase in the threshold voltage, sub threshold can be dramatically reduced. For these reason, leakage power consumption has become the dominant factor in the total power consumption. However, leakage power becomes critical in case of battery operated device such as cell phones, PDAs etc. Thus the technique for the low power is broadly classified into two types: state preserving logics and state destructive logic. In the former the logic state of the circuit is preserved whereas in the latter the logic state of the circuit is lost. My new approach retains the state of the logic circuit, thereby reducing the leakage power at the cost of increased delay.

Previous works

Here I review the previously proposed circuit level technique for sub threshold leakage power reduction.

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Sleep Transistor Approach

The most well-known traditional approach is sleep transistor approach (Mutoh *et al.,* 1995; Powell *et al.,* 2000). In sleep approach, additional PMOS transistor is placed between pull up network and power rails to cut off the supply during the active mode. Additional NMOS is placed between pull down network and ground to turn off the power rails during the idle mode. During sleep mode, sleep transistors are turned off and leakage current is suppressed. Thus output will be floating during the sleep mode, thus leading to destruction of state. Thus by cutting off the power, this technique can reduce the leakage power.

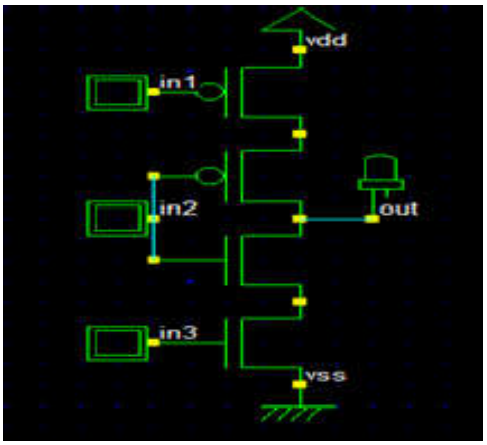

Fig. 1. Sleep transistor approach

Zigzag approach

Zigzag approach reduces the area overhead caused by the additional sleep transistor in sleep approach. By placing the alternate sleep transistor this overhead can be reduced by selecting the particular preselected input vector (Min *et al.,* 2003). In sleep mode, input of logic is "0" and each logic input reverses its state and the output is "1". Thus, the zigzag approach uses few sleep transistors than the sleep logic.

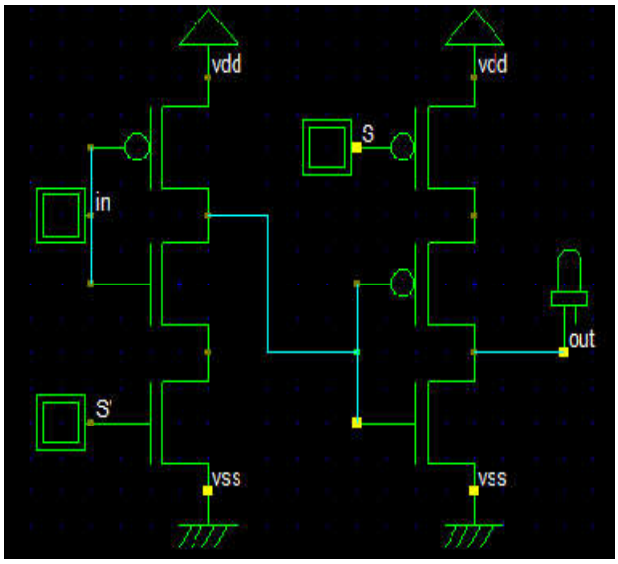

Fig. 2. Zigzag approach

Stack approach

Another low power reduction technique is the stack approach. It breaks down the existing transistor into two halves (Chen *et al.,* 1998). When two transistors are turned off simultaneously, sub threshold current is reduced with increased delay and area. Thus the logic state of the circuit is also maintained.

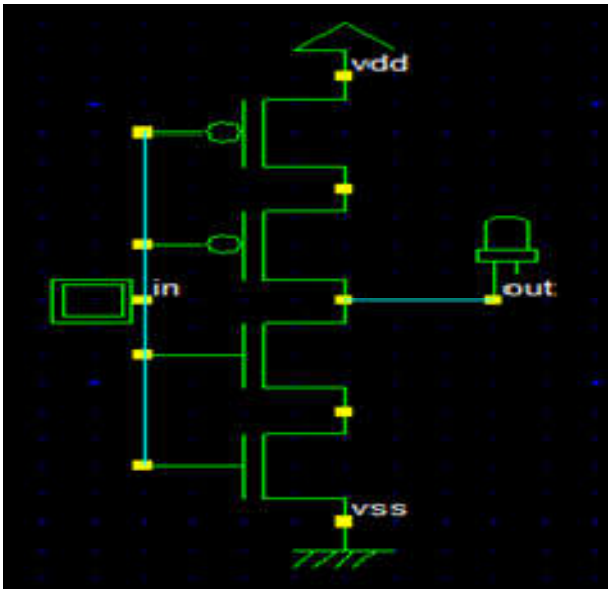

Fig. 3. Stack approach

Sleepy Stack approach

The sleepy stack is the combination of sleep and forced stack approach (Park *et al.,* 2004; Park, 2005). Sleepy approach can achieve low power leakage, but loses its logic state at its output. Forced stack reduces the leakage power by stacking of the transistor and also retain its state. It uses only low Vt transistors and so the leakage power saving is small. Thus by combining this two technique one can achieve (i) ultra low power leakage and (ii) retention of state. This technique divides existing transistor into two halves and then sleep transistors are placed parallel to one of the stacked transistor.

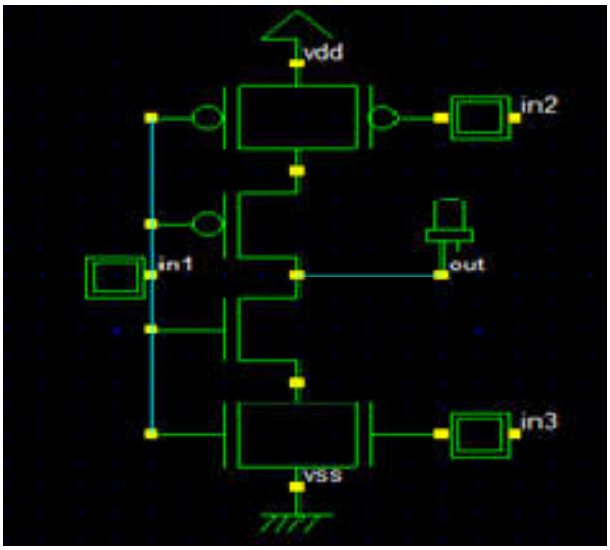

Fig. 4. Sleepy stack approach

Sleepy keeper

In this approach, PMOS transistor is placed parallel to the pull up sleep transistor and NMOS is placed parallel to pull down sleep transistor (Kim and Mooney, 2006). When in sleep mode, the NMOS is the only source of VDD to pull up network as the sleep transistor is turned off. When in active mode, PMOS is the only source of ground to pull down network as the sleep transistors is turned on. Due to the presence of sleep transistor, the resistance of the ON path increases thus decreasing the propagation delay. This approach retains the logic state of the circuit.

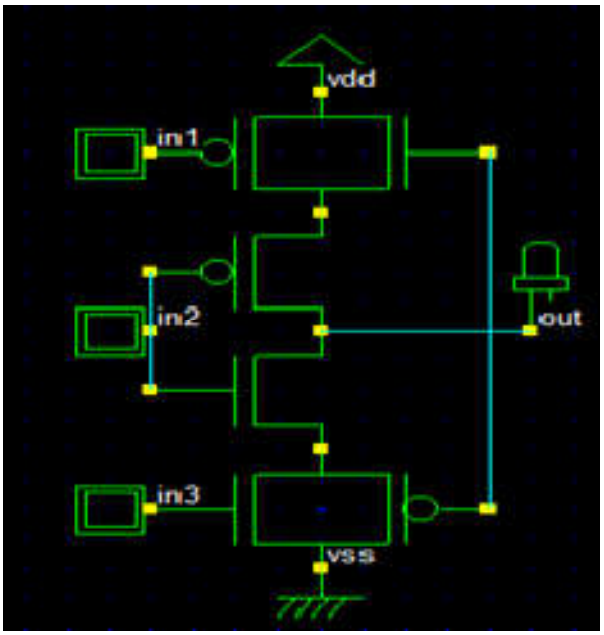

Fig. 5. Sleepy keeper approach

Proposed work

In this section we describe I new approach, sleepy stack with variable body biasing. This aims in reducing the sub threshold leakage current along with the retention of the logic state of the circuit. Sub threshold is the dominant among the all leakage currents and is caused by the minority carriers drifting from source to drain in the presence of weak inversion layer. Unlike stack approach, the original transistor is divided into two halves and the sleep transistors are placed parallel to one of the stacked transistor. Here the body of the sleep transistor is tied to the source of the PMOS/NMOS transistor in the pull up/Pull down network. During sleep mode, both the sleep transistors are turned off. So the body to source voltage of the pull up PMOS is higher than active mode. But the stack structure maintains the exact state of the circuit.

For the turned off transistor, the sub threshold leakage current can be expressed as,

$$Isub=Ie1n(Vgs-Vth-\gamma Vsb+\eta Vds)(1-e-VdsV\theta) \quad \ldots\ldots (1)$$

Where $I=\mu Cox(WL)V\theta 2e1.8$; n is sub threshold coefficient, Vθ is the thermal voltage, Vgs, Vth, Vs and Vds are the gate-to-source voltage, the zero-bias threshold voltage, the base-to-source voltage and the drain-to-source voltage, γ is the body-bias effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient. From the above equation it is evident that, leakage current decreases as Vsb increases. Thus as a result of body effect, threshold voltage increases which decreases the performance of the circuit. When in active mode, both the sleep transistor are turned on facilitating continuous flow of current, thus providing faster switching time. The performance is increased as the transistor is turned on, making the threshold voltage of the pull up PMOS lower again. The remaining PMOS/NMOS help to maintain the state during the sleep mode.

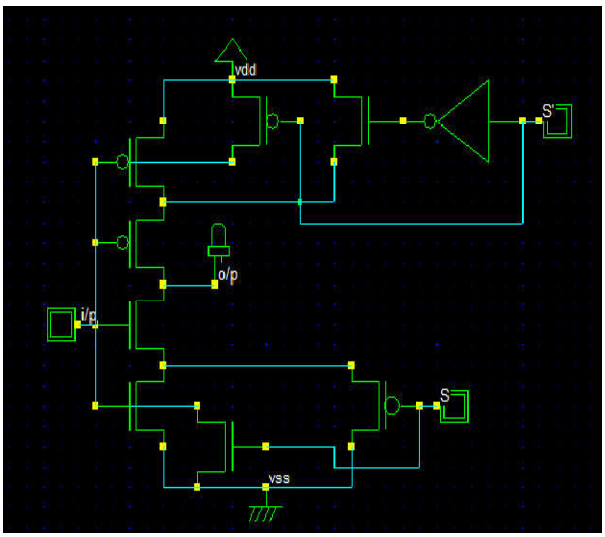

Fig. 6. Variable Body Biasing

Experimental Methodology

I compare the variable body bias technique with previously mentioned methods, namely, Base case, sleep, forced, sleepy stack and sleepy keeper approach. The comparison is made with respect to static power consumption, dynamic power consumption, propagation delay and area. This technique can be used to general logic circuits and memory. Inverter is chosen as the benchmark circuit. I use HSPICE for simulation purpose to estimate delay and power consumption. Area is estimated using MICROWIND tool. All the approaches are evaluated using low V_t transistors. The inverter uses W/L=3 for PMOS in the pull up network and W/L=1.5 for NMOS in the pull down network.

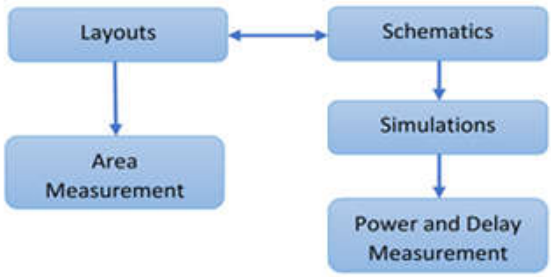

Fig. 7. Experimental Methodology

All the simulations are carried down at the room temperature of 27^0C, VDD= 1.2v, supply voltage of 2.5V.

Experimental Results

I measure static power dissipation, dynamic power dissipation, propagation delay and area for the five approaches namely, sleep, sleep stack, forced stack, sleepy keeper and base case with the proposed method. The simulation is performed using schematic entry and its corresponding test patterns are generated and its functionality is verified. fter verification the schematic file is converted into Verilog file, which gets converted into physical layout. Using the physical layout the area is found.

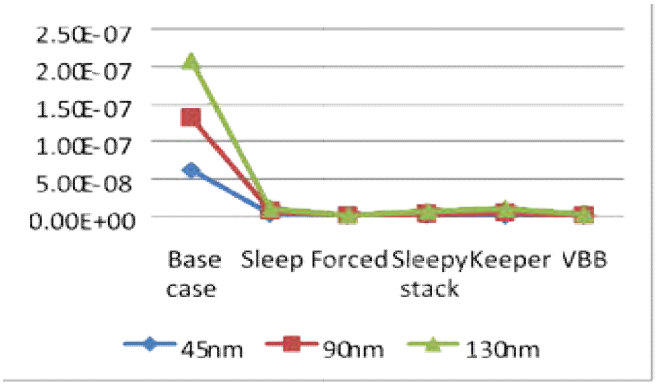

Fig. 8. Static power dissipation

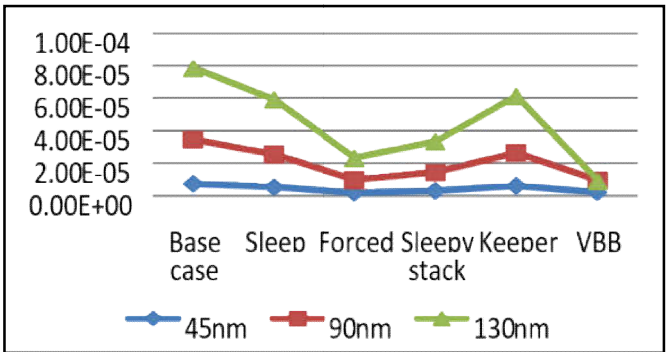

Fig. 9. Dynamic power dissipation

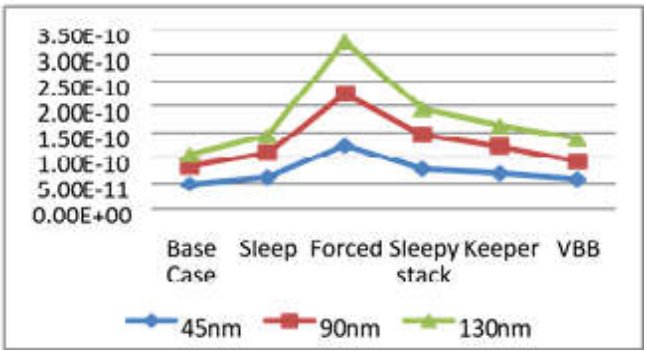

Fig. 10. Propagation delay

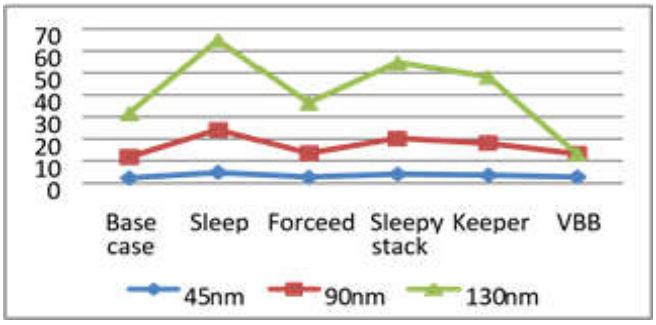

Fig. 11. Area Measurement

Table 1. Comparison table of existing and proposed leakage reduction techniques

45nm	Prop. Delay(s)	Static Power (W)	Dynamic Power (W)	Area (μm^2)
Base Case	2.29E-11	6.13E-08	7.29E-06	9.52
Sleep	4.77E-11	5.1E-09	5.81E-06	4.85
Forced stack	1.001E-10	1.3E-09	7.75E-06	2.73
Sleepy Stack	6.77E-11	2.47E-09	2.89E-06	4.09
Sleepy Keeper	5.22E-11	4.31E-09	5.99E-06	3.62
VBB	3.49E-11	1.11E-09	2.061E-06	2.87

Conclusion

Scaling down the device size and threshold voltage has lead to increase in the leakage power dissipation. My approach results in retention of the logic state as well as minimizing the leakage power.

Variable body biasing is the most efficient approach for reducing the leakage power with smallest delay and area. This approach is best suited for the basic logic circuits and memory.

REFERENCES

Chen, Z., M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," *International Symposium on Low Power Electronics and Design*, pp. 239-244, August 1998.

Kim, S. and V. Mooney, "The Sleepy Keeper Approach: Methodology, Layout and Power Results for a 4 bit Adder," Technical Report GITCERCS- 06-03,Georgia Institute of Technology, March 2006, http://www.cercs.gatech.edu/tech-reports/tr2006/git-cercs-06-03.pdf .

Min, K.S., H. Kawaguchi and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," *IEEE International Solid-State Circuits Conference*, pp. 400-401, February 2003.

Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multi threshold-Voltage CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 8, pp. 847-854, August 1995.

Park, J. "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005. [Online]. Available http://etd.gatech.edu/theses

Park, J.C., V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," *Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation*, pp. 148-158, September 2004.

Powell, M., S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijay kumar, "Gated Vdd: A Circuit Technique to Reduce Leakage in deep submicron Cache Memories," *International Symposium on Low Power Electronics and Design*, pp. 90-95, July 2000

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